DTU Introduces “Partial Dynamic Reconfiguration”

On April 27th, the DTU Center for Research and Development held a symposium on “**Partial Dynamic Reconfiguration**” *(PDR)*. Mr. Nguyen Trong Tuan, System Design Manager from the Vietnam division of Acronics Systems, answered questions from the DTU faculty and students about digital design.

Mr. Nguyen Trong Tuan introduces “Partial Dynamic Reconfiguration”

Since 2010, Mr. Tuan has spent most of his time researching High Performance Computing on the FPGA Platform and Reconfiguration Systems. He has also taken part in various key projects and his research has been published nationally and internationally. His papers include “The DDR2/DDR3-based Ultra-Rapid Reconguration Controller”, in ICCE 2012, and “The Design and Implementation of the 32- bit RISC Microprocessor on an FPGA Platform”, in the Science and Technology Magazine of Danang University in 2012.

With his research experiences, Mr. Tuan has introduced several developed systems on FPDA with its advantages such as: allowing adapting special applications from embedded system and digital system, rapid processing, high performance in such fields as aviation, cosmology, national defense, telecommunication networks and high - speed pinelines.

Mr. Tuan said: “*With PDR on the Xilinx FPGA, we are able to adapt to changes required by the system itself, by configuring a simultaneous bit stream, while other components of the system are already active. PDR’s advantages include reducing FPGA resource usage, energy consumption, propagation delays and hacking*”.

During the symposium, many questions were answered by Mr.Tuan relating to PDR, the technology in general, SoC architecture on the PDR FPGA platform and future developments.

(Board of Website Editors)